WHAT IS CLAIMED IS:

1. A system architecture of semiconductor manufacturing equipment, comprising:

degas chamber(s), wherein said degas chamber(s) are integrated to the conventional pass-through chamber location.

2. The system architecture of claim 1, wherein the system has 3 swaps each for buffer robot and transfer robot.

3. A system for depositing Cu barrier and seed layers on a semiconductor wafer, comprising:

a front opening unified pod(s);

a single wafer loadlock chamber(s);

a degas chamber(s), wherein said degas chamber is integrated to a pass-through chamber;

a preclean chamber(s);

a Ta or TaN process chamber(s); and

a Cu process chamber(s).

4. The system of claim 3, wherein said degas chamber is selected from the group consisting of IR lamps degas chamber, resistively heated pedestal degas chamber, IR

lamps degas chamber with cool-down pedestal, and resistively heated pedestal degas chamber with integrated cool-down station.

5. A method of depositing Cu barrier and seed layers on a semiconductor wafer using the system of claim 3, comprising the steps of:

loading said wafer to the degas chamber from the front opening unified pod through the single wafer loadlock chamber;

performing degas processing on said wafer in said degas chamber;

removing native oxide from said wafer in the preclean chamber;

depositing Ta or TaN on said wafer in the Ta or TaN process chamber;

passing the processed wafer through the degas chamber;

depositing Cu layer on said wafer in the Cu process chamber: and

transferring the processed wafer from the Cu process chamber to the front opening unified pod through the single wafer loadlock chamber, thereby obtaining a wafer with Cu barrier and seed layer deposition.

6. The method of claim 5, wherein said method processes more than 100 wafers per hour.